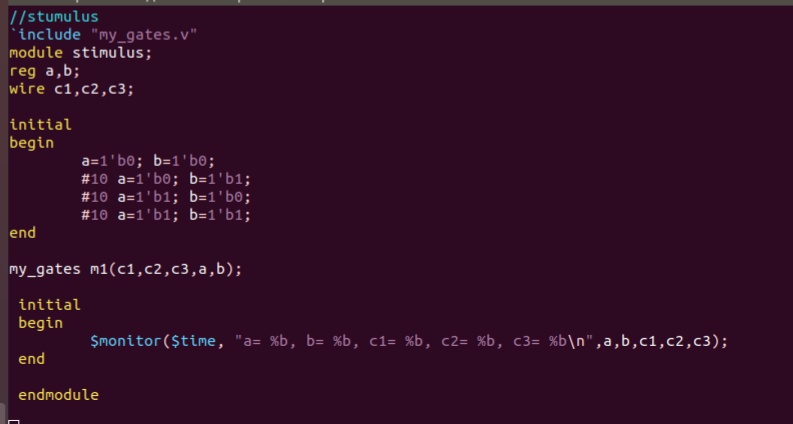
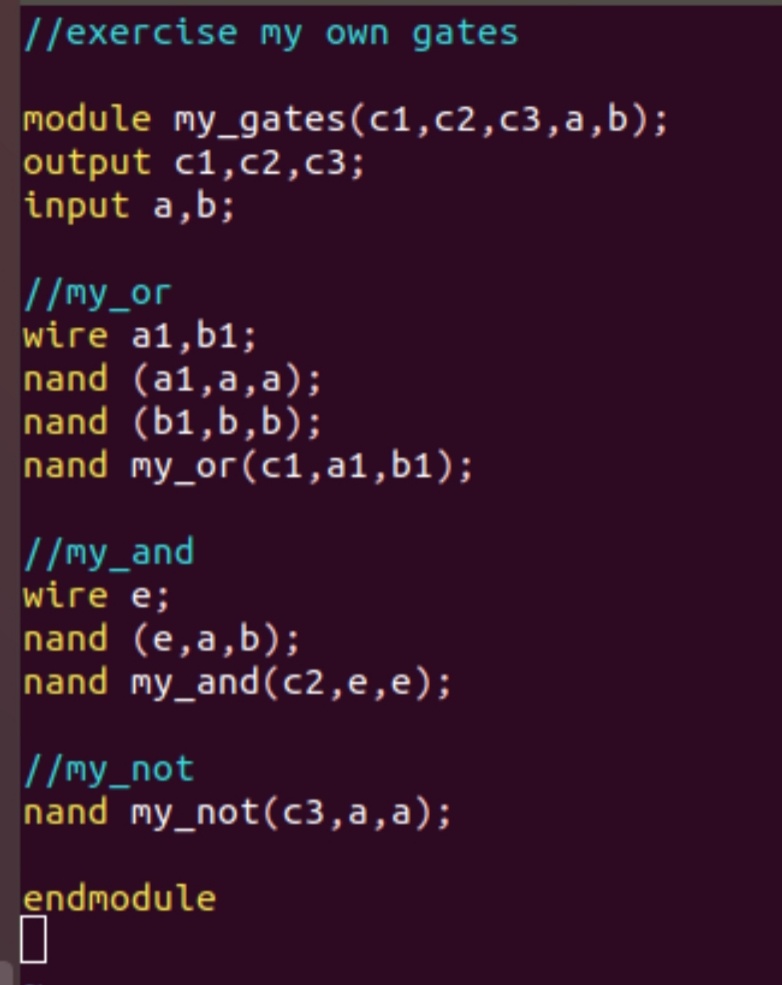
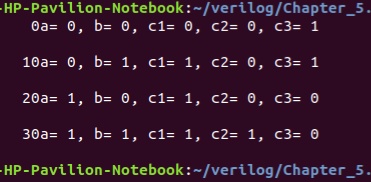
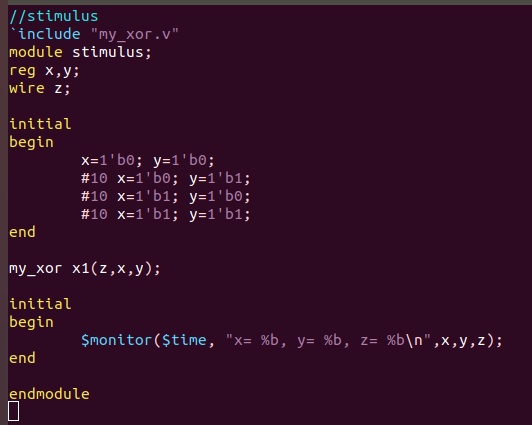
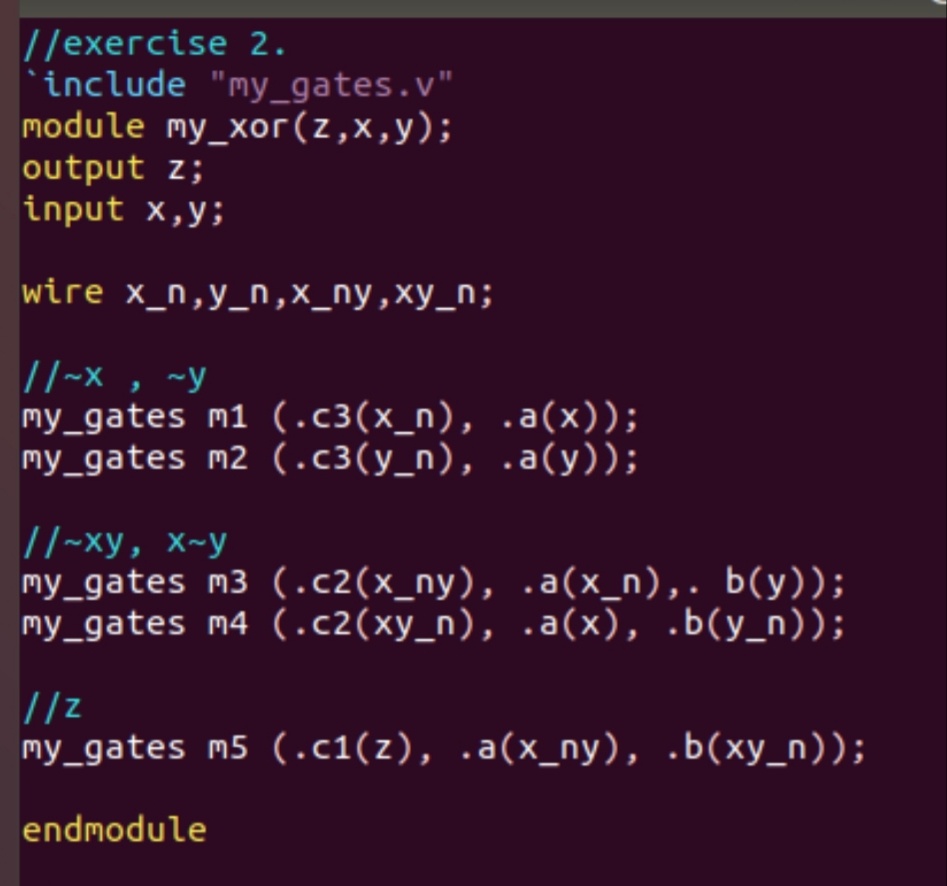
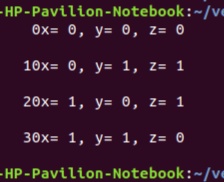
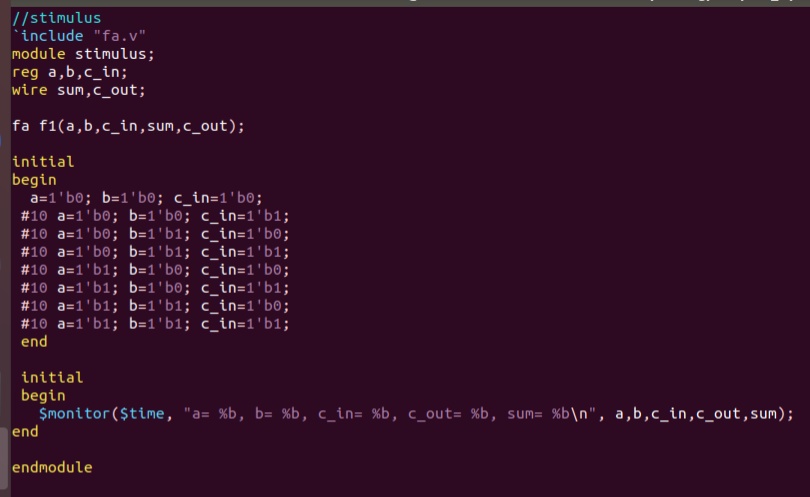
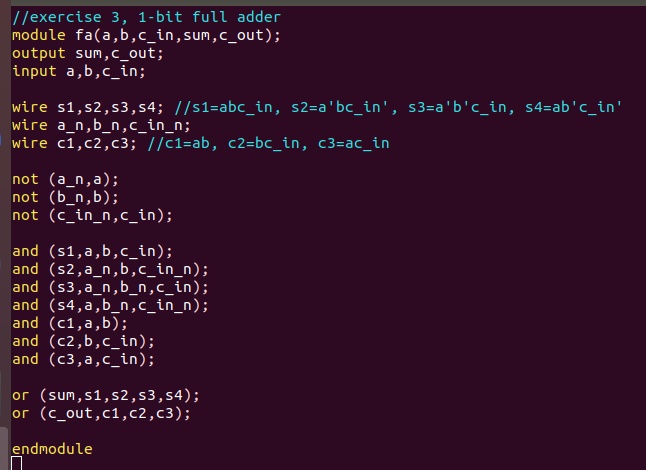
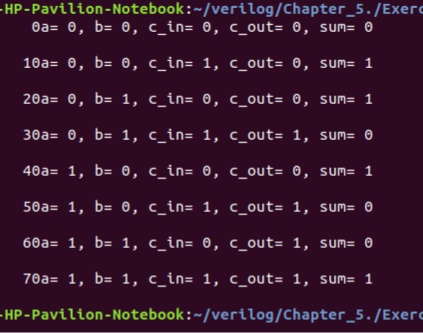
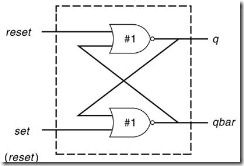
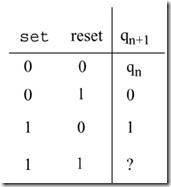
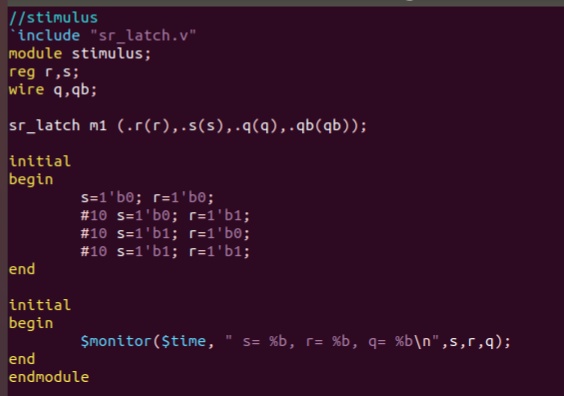
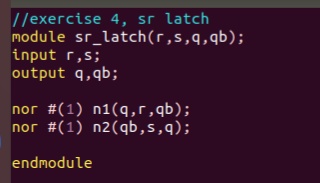
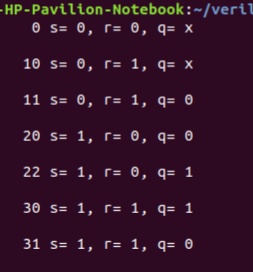
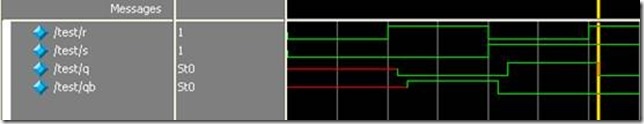
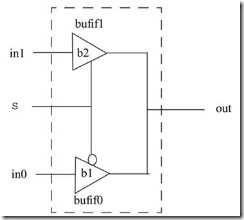
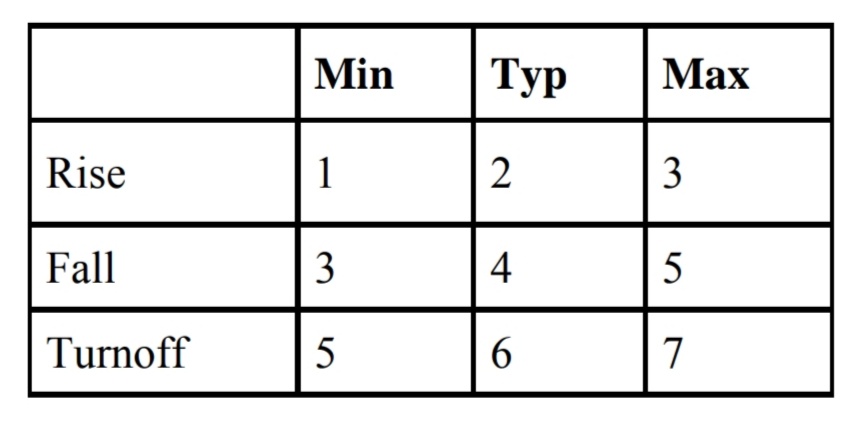
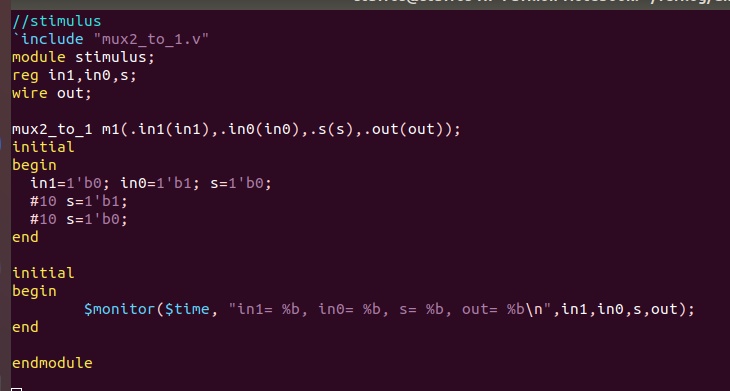
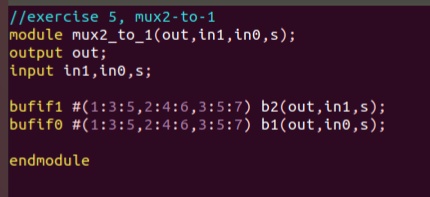
**Chapter 5. Gate-level Modeling  
  
5.4 Exercises**  
1. Create your own 2-input Verilog gates called my\_or, my\_and and my\_not from 2-input nand gates. Check the functionality of these gates with a stimulus module.  
  
**Պատասխան`**  
  
**Արդյունքը** `  
  
  
2. A 2-input xor gate can be built from my\_and, my\_or and my\_not gates. Construct an xor module in Verilog that realizes the logic function, z=xy’+x’y. Inputs are x and y, and z is the output. Write a stimulus module that exercises all four combinations of x and y inputs.  
  
**Պատասխան**`  
  
  
**Արդյունքը**`  
  
  
3. The 1-bit full adder described in the chapter can be expressed in a sum of products form.  
  
**sum=a.b.c\_in+a’.b.c\_in’+a’.b’.c\_in+a.b’c\_in’  
  
c\_out=a.b+b.c\_in+a.c\_in**  
Assuming a,b,c\_in are the inputs and sum and c\_out are the outputs, design a logic circuit to implement the 1-bit full adder, using only and, not ,and or gates. Write the Verilog description for the circuit. You may use up to 4-input Verilog primitive and and or gates. Write the stimulus for the full adder and check the functionality for all input combinations.  
  
**Պատասխան`**  
  
**Արդյունքը**`  
  
  
4. The logic diagram for an RS latch with delay is shown below.  
  


Write the Verilog description for the RS latch. Include delays of 1 unit when instantiating the nor gates. Write the stimulus module for the RS latch, using the following table, and verify the outputs.  
  
  
**Պատասխան`**  
**Արդյունքը`**  
  
  
5. Design a 2-to-1 multiplexer using bufif0 and bufif1 gates as shown below.  
  


The delay specification for gates b1 and b2 are as follows:  
  
  
Apply stimuls and test the output values.  
  
**Պատասխան`**  
  
**Արդյոյնքը`**  
